CS-00-025

DOUBLE-LAYERED LOW DIELECTRIC CONSTANT DIELECTRIC DUAL DAMASCENE METHOD

RELATED PATENT APPLICATION

U.S. Patent Application Serial # 09726657 (CS-00-024) to Q.S. Fong et al., filed November 30, 2000, now US Patent 6,406,994.

L, J.W-E, 6/22/2004

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of metallization in the fabrication of integrated circuits, and more particularly, to a method of dual damascene metallization using low dielectric constant materials in the manufacture of integrated circuits.

(2) Description of the Prior Art

The damascene or dual damascene process has become a future trend in integrated circuit manufacturing, especially in the copper metallization process. These processes are discussed in ULSI Technology, by Chang and Sze, The McGraw Hill Companies, Inc., NY, NY, c. 1996, pp. 444-445. Low dielectric constant materials have been proposed as the dielectric materials in order to reduce capacitance. In